REMARKS

Claims 1, 4-9, 11, 13-16, and 18-23 are pending. By this Amendment, claims 2-3, 10, 12 and 17 are canceled without prejudice or disclaimer and claims 1, 4, 6-9, 11, 14, 16 and 23 are amended. Reconsideration in view of the above amendments and following remarks is respectfully requested.

Claims 1-6 and 11-13 were rejected under 35 U.S.C. § 102(b) over Mueller et al. (U.S. Patent 6,320,780). The rejection is respectfully traversed.

Mueller et al. do not disclose or suggest biasing the other of the precharged first bitline and the precharged second bitline (i.e. the bitline not charge sharing with the capacitance of the memory cell) to decrease a voltage level of the biased bitline below the precharge voltage in order to increase a refresh period, as recited in claim 1. As disclosed by Mueller et al. in column 1, lines 45-53, ideally the reference bitline (i.e. the bitline not coupled to the memory cell's capacitor) remains at the predefined voltage level (e.g. equalization voltage or v_{bleq}). Although Mueller et al. disclose in column 2, lines 1-4, that the reference bitline voltage increases or decreases due to intra-bitline coupling, Mueller et al. do not disclose or suggest biasing the reference bitline to decrease its voltage level below the equalization voltage. Accordingly, Mueller et al. do not anticipate or render obvious claim 1.

Claims 2-6 recite additional features of the invention and are allowable for the same reasons discussed above with respect to claim 1 and for the additional features recited therein.

Mueller et al. do not disclose or suggest biasing a selected one of the precharged bitlines to decrease a voltage level of the biased bitline below the precharge voltage so as to increase a refresh period, as recited in claim 11. As discussed above, Mueller et al. disclose that the bitlines are precharged to a predefined voltage level (e.g. equalization voltage or v_{bleq}) and that the reference bitline voltage may increase or decrease due to intra-bitline coupling, but do not disclose or suggest biasing the bitline to decrease its voltage level.

Claims 12 and 13 recite additional features of the invention and are allowable for the same reasons discussed above with respect to claim 11 and for the additional features recited therein.

Reconsideration and withdrawal of the rejection over Mueller et al. are respectfully requested.

Claims 7-10 were rejected under 35 U.S.C. § 102(b) over Yamada et al. (U.S. Patent 5,375,095). The rejection is respectfully traversed.

Yamada et al. do not disclose or suggest asserting a bias signal corresponding to the wordline for decreasing a potential of a reference bitline, as recited in claim 7. As disclosed in column 10, lines 57-58, the selected wordline 3 is raised to the high level potential, its potential is not decreased. Accordingly, Yamada et al. do not anticipate or render obvious claim 7.

Claims 1-10 recite additional features of the invention and are allowable for the same reasons discussed above with respect to claim 7 and for the additional features recited therein.

Claims 14-18 were rejected under 35 U.S.C. § 102(b) over Kumanoya et al. (U.S. Patent 4,933,907). The rejection is respectfully traversed.

Kumanoya et al. do not disclose or suggest a bias circuit configured and arranged to decrease a potential of the reference bitline to increase a refresh period in a semiconductor memory device, as recited in claim 14. Kumanoya et al. disclose in column 18, lines 10-25, that the set time set in the timer 110 does not exceed the capability of the refresh time of the memory cell, the power consumption can be decreased. The example Kumanoya et al. provide for accomplishing this power consumption reduction is to controlling the level of the bitline precharging potential V_{PL}. Kumanoya et al. do not disclose or suggest decreasing a potential of a reference bitline (i.e. a bitline that is precharged, but not selected to share a charge with the memory cell) to increase a refresh period. Therefore, Kumanoya et al. do not anticipate or render obvious claim 14.

Claims 15-18 recite additional features of the invention and are allowable for the same reasons discussed above with respect to claim 14 and for the additional features recited therein.

Reconsideration and withdrawal of the rejection over Yamada et al. are respectfully requested.

Applicants appreciate the indication that claims 19-23 define patentable subject matter. However, in view of the above amendments and remarks, Applicants respectfully submit that all claims are allowable and that the entire application is in condition for allowance.

Should the Examiner believe that anything further is desirable to place the application in better condition for allowance, the Examiner is invited contact the undersigned at the telephone number listed below.

Respectfully submitted,

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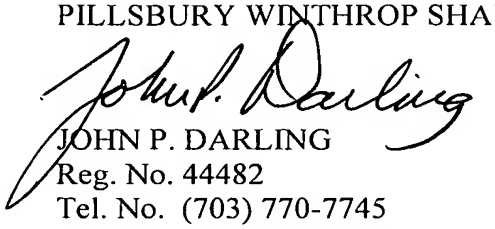

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